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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,818	11/29/2001	Eiji Furukawa	122.1476	9741

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EXAMINER	
ROSARIO, DENNIS	
ART UNIT	**PAPER NUMBER**
2624	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,818	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Dennis Rosario	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE 5/12/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11,12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 12, 2006 has been entered.

Response to Amendment

2. The amendment was received on May 12, 2006. Claims 1-9,11,12,14 and 15 are pending.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9,11,12,14 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Miura et al. (US Patent 5,847,968 A).

Regarding claim 1, Miura et al. discloses a logic drawing entry apparatus, comprising:

a) a means for creating an inter-drawing connection diagram file (fig. 5D) which describes interrelation in a plurality of drawing sheets (as shown to the right in fig. 5D); and

b) inter-drawing indication means for indicating, on one screen (as shown in fig. 8), a plurality of the miniaturized drawing sheets (as shown in fig. 8 as two chips on the top-left side of fig. 8 and a "L" shaped circuit board located in the bottom left of fig. 8; in light of page 3, paragraph [0009] of the specification, the two chips and the circuit board are interpreted as miniaturized drawing sheets because the two chips and circuit boards are outlined as is done in fig. 5B, label: OUTLINE for the two chips and in fig. 8 as a L-shaped outline of the circuit board as also shown in fig. 22B: CIRCUIT BOARD OUTLINE ENLARGED), said miniaturized drawing sheets are connected by nets (as shown in fig. 11A by the dashed lines), according to the description in the inter-drawing diagram file which has been created.

Regarding claim 2, Miura et al. discloses the logic drawing entry apparatus of claim 1, further comprising:

a) inter-drawing diagram editing means (fig. 3,num. S4008) for implementing editing works on each of a plurality of said drawing sheets when the plurality of said drawings are indicated on one screen.

Regarding claim 3, Miura et al. discloses the logic drawing entry apparatus of claim 2, wherein said inter-drawing connection diagram editing means, further, modifies the position (in fig. 3,num. S4004) of each drawing sheet on an indication screen.

Regarding claim 4, Miura et al. discloses the logic drawing entry apparatus of claim 2, wherein said inter-drawing connection-diagram editing means, further, modifies the attributes (in fig. 3,num. S4005) of each drawing sheet on an indication screen.

Regarding claim 5, Miura et al. discloses the logic drawing entry apparatus of claim 1, further comprising:

a) inter-drawing connection counting means (fig. 5D, label: NUMBER OF CONSTITUTING POINTS) for counting the number of connections (as shown in the right of fig. 5D as small circles) between a plurality of said drawing sheets about symbols included in a plurality of said drawing sheets; and

b) a net connection relation drawing means (fig. 5C) for drawing net connection relations (as shown to the right of fig. 5C, labels A and B) between said drawings sheets based on the number of inter-drawing connections counted by said inter-drawing connection counting means.

Regarding claim 6, Miura et al. discloses the logic drawing entry apparatus of claim 5, wherein said net connection relation drawing means has a function of modifying (as shown in fig. 31, label: "ROUTING PATTERN CREATED") the indications of the nets (as shown in fig. 31, numerals 2410-2413 in relation to fig. 31, numerals 2420 that are shown four times) according to said number of inter-drawing connections (since the routing pattern created uses all the elements of fig. 5D that includes NUMBER OF CONSTITUTING POINTS that corresponds to the claimed said number of inter-drawing connections).

Regarding claim 15, Miura et al. discloses the logic drawing entry apparatus of claim 1, wherein said plurality of miniaturized drawing sheets are drawn in a shape of a block diagram (as shown in fig. 47A which is a diagram of blocks; in another interpretation since each circuit component has an associated outline then each outline in interpreted as a block that can form a circuit or diagram of blocks).

6. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Otaguro (US Patent 6,966,045 B2).

Regarding claim 14, Otaguro discloses a logic drawing entry apparatus for processing of drawings in which hierarchic symbols, which is an expression of the logic circuit at a certain hierarchical level as the symbol, having a plurality of pins are described, the logic drawing entry apparatus comprising:

a) a hierarchic symbol drawing means for drawing (fig. 16,num. S10) by dividing said hierarchic symbols (as shown in fig. 15,numerals r1 and r2); and

b) a net drawing means for drawing nets (fig. 16,num. S27 as shown in fig. 15 as a line that connects r1 and r2 together using black dots) for individual symbols which have been drawn.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. (US Patent 5,847,968 A) in view of Merchant et al. (US Patent 6,490,712 B1).

Regarding claim 7, Miura et al. does not teach the limitation of claim 7 but teaches that "names are set...and how to set them is left to a designer" in col. 12, lines 50-53. Thus, Miura et al. suggests to one of ordinary skill in the art to set names in any fashion desired.

Merchant et al. teaches a method of setting names as shown in fig. 1B, label: Logical Name and the remaining limitation of:

a) drawing name modifying means (fig. 3A, num. 330) for selecting a plurality of said drawings sheets and modifying the name of said plurality of drawing sheets, in ascending or descending order.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Miura et al.'s teaching of setting a name with Merchant et al.'s teaching of fig. 3A,num. 330, because Merchant et al.'s teaching of fig. 3A, num. 330 makes finding names easier.

Regarding claim 8, Merchant et al. of the combination teaches the logic entry apparatus of claim 7, wherein said drawing name modifying means, further, designates intervals (since fig. 3A uses alphanumeric sort via numbers) between the names of said plurality of drawing sheets.

9. Claims 9,11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al. (US Patent 5,218,551 A) in view of Eldridge et al. (US Patent 6,429,029 B1).

Regarding claim 9, Agrawal et al. teaches a logic drawing entry apparatus for processing of drawings in which are indicated a plurality of symbols, and nets expressing connection relations between the symbols, the logic drawing entry apparatus comprising:

a) symbol selecting for selecting ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55.) symbols ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 symbols or "segments" in col. 17, line 55. Note that a segment is a groups of blocks as mentioned in col. 10, line 2. Thus, fig. 10a shows 4 segments labeled "Precinct 1" through "Precinct 4.") to be moved ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 symbols or "segments" in col. 17, line 55 to be "move[d]" in col. 17, line 56.) and positions ("move class" in col. 17, line 57 is a means for "chos[ing]" in col. 17, line 55 positions or ends: "one end...to the other" in col. 17, line 63.) to which the selected symbols are to be moved,

b) symbol moving means (Fig. 7,num. 718 interchanges segments where interchanging is a form of moving or a "move" in col. 17, line 1.) for moving said selected symbols (segments) to said positions (or ends: "one end...to the other" in col. 17, line 63. Thus, using fig 10a, a segment at one end labeled "Precinct 2" can be interchanged with other segments, labeled "Precinct 2" through "Precinct 4.");

c) symbol swapping means for swapping positions of said selected symbols with the positions to which said selected symbols are to be moved when symbols, other than said selected symbols, exist at the positions to which said selected symbols are to be moved (This limitation has been addressed in paragraph c), above. Note that a swap or interchange of an individual block instead of a segment as shown in fig. 10a, num. 874 is swapped or interchanged with 872 of fig. 10a with the result of the swap or interchange of numerals 872 and 874 is shown in fig. 10b.), and

d) net redrawing means (fig. 1,num. 800) for redrawing nets (as shown in figs, 10a and 10b) for said selected symbols (segments) after the movement or swap while keeping the connection relations between said selected symbols before the movement (as can clearly be shown when comparing the connections or lines of segments/blocks between figures 10a and 10b.).

Agrawal et al. does not teach a means for selecting but does teach that a user can input values into a simulated annealing method which is "well known" in col. 13, lines 47,48 and that a "user" in col. 14, line 8 can input values into the method. However, Agrawal et al. does not show how a user can input the values into the method. Thus, Agrawal et al. suggests to one of ordinary skill in the art that there are other teachings available about simulated annealing that can be used with the invention.

Eldridge et al. teaches "simulated annealing" in col. 12, line 12 method and the remaining limitation of means for selecting as shown in fig. 9, numerals 916 and 918. Note that fig. 9, numerals 916 and 918 are interpreted as a means for selecting user preferences as shown in fig. 7,num. 614.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Agrawal et al.'s teaching of inputting values into the simulated annealing method with Eldridge et al.'s teaching of means for selecting, because Eldridge et al.'s means for selecting is well known to one of ordinary skill in the art.

Regarding claim 11, Agrawal et al. of the combination teaches the logic drawing entry apparatus of claim 9, further comprising:

a) an arranging means ("global net" in col. 14, line 22 an shown in fig. 11 as a grid or Net 625.) for arranging a plurality of selected symbols (as shown in fig. 10a and 10b as smaller squares where numerals 872 and 874 represent the smaller squares.) on a drawing in a column or a row ("row and column...for the precincts...[as shown in fig. 10a and 10b.]).

Regarding claim 12, Agrawal et al. of the combination teaches the logic drawing entry apparatus of claim 11, wherein said arranging means, further, designates:

a) intervals ("distance" in col. 17, line 67) between symbols (or "first segment...[and]...second segment" from col. 17, line 68 to col. 18, line 1.).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario whose telephone number is (571) 272-7397. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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